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SMART & BIGGAR
2200 - 650 WEST GEORGIA STREET
BOX 11560, VANCOUVER CENTRE
VANCOUVER, BC V6B4N8
CANADA

EXAMINER	
DUONG, FRANK	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/475,308	Applicant(s) MONTUNO ET AL.	
	Examiner Frank Duong	Art Unit 2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,71 and 72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 71-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to the amendment dated 5/20/2004. Original claims 1-10, amended claims 11-21 and newly added claims 71-72 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-21 and claims 71-72 are rejected under 35 U.S.C. 102(b) as being anticipated by Srinivasan et al (Faster IP Lookups using Controlled Prefix Expansion, pages 1-10, ACM, June 1998) (hereinafter "Srinivasan").

Regarding **claim 1**, in accordance with Srinivasan reference entirety, Srinivasan discloses a method of encoding a plurality of predefined codes into a search key (controlled prefix expansion) (page 4, section 4.1), the method comprising:

a) producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predetermined code in said plurality of said pre-defined codes such that said bit positions are arrange by the lengths of said possible bit combinations and by numeric value of said possible bit combinations (*page 4, Figure 1 and the description on left column related prefix expansion);* and

b) setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes (*page 4, Figure 1 and the description on right column related to prefix capture*).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales discussed above), Srinivasan further discloses wherein producing comprises arranging

said bit positions in order by ascending lengths of corresponding said possible bit combinations (*see page 4, Figure 1; Srinivasan shows expanded prefixes are arranged bit positions (00 - 10000000) in order by ascending lengths (Length 2 - Length 7)*)

Regarding **claim 3**, in addition to features recited in base claim 2 (see rationales discussed above), Srinivasan further discloses wherein producing comprises further arranging said bit positions in order by ascending numeric value of corresponding said possible bit combinations (*see page 4, Figure 1; Srinivasan shows expanded prefixes are arranged bit positions (00 - 10000000)).*

Regarding claim 4, in addition to features recited in base claim 1 (see rationales discussed above), Srinivasan further discloses producing a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet (*see page 5, Figure 3; pointer from root to leaves nodes*).

Regarding **claim 5**, in addition to features recited in base claim 1 (see rationales discussed above), Srinivasan further discloses wherein producing comprises producing a plurality of PNBAS (expanded prefixes), each PNBA corresponding to a sub-group of bits of said pre-defined codes (*see page 4, Figure 1; Expanded prefixes*).

Regarding **claim 6**, in addition to features recited in base claim 5 (see rationales discussed above), Srinivasan further discloses producing an External Subtree Root Bit Array (ESRBA) (length) for each PNBA (prefix), said ESRBA having bit positions corresponding to possible further subgroups of bits (leaf) of said pre-defined trees (*see page 4, Figure 2; root and leaf and page 5, Figure 3; Expanded trie*).

Regarding **claim 7**, in addition to features recited in base claim 6 (see rationales discussed above), Srinivasan further discloses producing a plurality of pages, each page comprising a plurality of PNBA-ESRBA pairs (prefix, length) (*see page 5, discussion reference to expanded database of Figure 1*).

Regarding **claim 8**, in addition to features recited in base claim 6 (see rationales discussed above), Srinivasan further discloses producing a next hop array associating bit positions of said PNBA which have active bits with routing

information for use by a router to route a packet (*see page 5, Figure 3; pointer from root to leaves nodes*).

Regarding **claim 9**, in addition to features recited in base claim 8 (see rationales discussed above), Srinivasan further discloses associating with each of said PNBAS a next hop pointer pointing to a position in said next hop array at which next hop information associated with a first active bit of said PNBA is located *(*see page 5, Figure 3; pointer from root to leaves nodes*)*.

Regarding **claim 10**, in addition to features recited in base claim 9 (see rationales discussed above), Srinivasan further discloses arranging said plurality of respective pages, each page comprising a PNBA an associated ESRBA, an associated next bop pointer and a next page pointer pointing to a next page in said plurality of respective pages to be searched *(*see page 5, Figure 3; pointer from root to leaves nodes*)*.

Regarding **claim 11**, in accordance with Srinivasan reference entirety, Srinivasan discloses an apparatus (*page 2, software/Hardware related discussion*) for encoding a plurality of predefined codes into a search key, the apparatus (processor or forwarding engine) comprising:

a) means (processor) for producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predetermined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said bit

combinations (*page 4, Figure 1 and the description on left column related prefix expansion)*; and

b) means (processor) for setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes (p*age 4, Figure 1 and the description on right column related to prefix capture*).

Regarding **claim 12**, in accordance with Srinivasan reference entirety, Srinivasan discloses apparatus for encoding a plurality of predefined codes into a search key (*page 2, software/hardware related discussion*), the apparatus comprising a processor circuit (*processor or forwarding engine*) configured to:

a) produce a Prefix Node Bit Array (RNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predefined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations (*page 4, Figure 1 and the description on left column related prefix expansion)*, and

b) set bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes (p*age 4, Figure 1 and the description on right column related to prefix capture*).

Regarding **claim 13**, in addition to features recited in base claim 12 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to arrange said bit positions in order by ascending lengths of corresponding said possible bit combinations (*see page 4, Figure 1; Srinivasan*

shows expanded prefixes are arranged bit positions (00 - 10000000) in order by ascending lengths (Length 2 - Length 7)).

Regarding **claim 14**, in addition to features recited in base claim 13 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to further arrange said bit positions in order of ascending numeric value of corresponding said possible bit combinations (*see page 4, Figure 1; Srinivasan shows expanded prefixes are arranged bit positions (00 - 10000000))*.

Regarding **claim 15**, in addition to features recited in base claim 12 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet.

Regarding **claim 16**, in addition to features recited in base claim 12 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a plurality' of PNBAS, each PNBA corresponding to a subgroup of bits of said pre-defined codes (*see page 4, Figure 1; Expanded prefixes*).

Regarding **claim 17**, in addition to features recited in base claim 16 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce an External Subtree Root Bit Array (ESRBA) for each PNBA said ESRBA having bit positions corresponding to possible further

subgroups of bits of said pre-defined codes (*see page 4, Figure 2; root and leaf and page 5, Figure 3; Expanded trie*).

Regarding **claim 18**, in addition to features recited in base claim 17 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a plurality of pages, each page comprising a plurality of PNBA-ESRBA pairs (prefix, length) (*see page 5, discussion reference to expanded database of Figure 1*).

Regarding **claim 19**, in addition to features recited in base claim 17 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a next hop array associating bit positions of said PNBA which have active bit with routing information for use by a router to route a packet.

Regarding **claim 20**, in addition to features recited in base claim 19 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to associate with each of said PNBAS a next hop pointer pointing to a position in said next hop array at which next hop information associated with a first active bit of said PNBA is located (*see page 5, Figure 3; pointer from root to leaves nodes*).

Regarding **claim 21**, in addition to features recited in base claim 20 (*see rationales discussed above*), Srinivasan further discloses wherein said processor is configured to arrange said plurality of PNBAS into a plurality of respective pages, each page comprising a PNBA, an associated ESRBA, an associated next hop pointer and a next page pointer pointing to a next page in said plurality

of respective page to be searched (*see page 5, Figure 3; pointer from root to leaves nodes*).

As per **claims 71-72**, they're rejected by the same rationales applied to claim 1.

3. Claims 1-21 and 71-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Srinivasan (USP 6,011,795).

Regarding **claim 1**, in accordance with Srinivasan reference entirety, Srinivasan discloses a method of encoding a plurality of predefined codes into a search key (controlled prefix expansion), the method comprising:

a) producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predetermined code in said plurality of said pre-defined codes such that said bit positions are arrange by the lengths of said possible bit combinations and by numeric value of said possible bit combinations (*columns 7-8, Figures 5-8 and the description related prefix expansion);* and

b) setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes (*column 8, Figures 5-8 and the description on right column related to prefix capture*).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales discussed above), Srinivasan further discloses wherein producing comprises arranging

said bit positions in order by ascending lengths of corresponding said possible bit combinations (*see Figure 8*).

Regarding **claim 3**, in addition to features recited in base claim 2 (see rationales discussed above), Srinivasan further discloses wherein producing comprises further arranging said bit positions in order by ascending numeric value of corresponding said possible bit combinations (Figure 8*)*.

Regarding **claim 4**, in addition to features recited in base claim 1 (see rationales discussed above), Srinivasan further discloses producing a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet (*see Figure 8; Link or Figure 9; pointer from root to leaves nodes*).

Regarding **claim 5**, in addition to features recited in base claim 1 (see rationales discussed above), Srinivasan further discloses wherein producing comprises producing a plurality of PNBAS (expanded prefixes), each PNBA corresponding to a sub-group of bits of said pre-defined codes (*see Figure 8; Expanded prefixes*).

Regarding **claim 6**, in addition to features recited in base claim 5 (see rationales discussed above), Srinivasan further discloses producing an External Subtree Root Bit Array (ESRBA) (length) for each PNBA (prefix), said ESRBA having bit positions corresponding to possible further subgroups of bits (leaf) of said pre-defined trees (*Figure 9; Expanded trie*).

Regarding **claim 7**, in addition to features recited in base claim 6 (see rationales discussed above), Srinivasan further discloses producing a plurality of

pages, each page comprising a plurality of PNBA-ESRBA pairs (prefix, length) (*see Figure 8*).

Regarding **claim 8**, in addition to features recited in base claim 6 (see rationales discussed above), Srinivasan further discloses producing a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet (see Figure 9; pointers from root to leaves nodes).

Regarding **claim 9**, in addition to features recited in base claim 8 (see rationales discussed above), Srinivasan further discloses associating with each of said PNBAS a next hop pointer pointing to a position in said next hop array at which next hop information associated with a first active bit of said PNBA is located (*see Figure 9; pointers from root to leaves nodes*).

Regarding **claim 10**, in addition to features recited in base claim 9 (see rationales discussed above), Srinivasan further discloses arranging said plurality of respective pages, each page comprising a PNBA an associated ESRBA, an associated next bop pointer and a next page pointer pointing to a next page in said plurality of respective pages to be searched *(see Figure 9; pointers from root to leaves nodes).*

Regarding **claim 11**, in accordance with Srinivasan reference entirety, Srinivasan discloses an apparatus (*Figure 13*) for encoding a plurality of predefined codes into a search key, the apparatus (*processor or forwarding engine*) comprising:

a) means (processor) for producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predetermined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations (*columns 7-8, Figures 5-8 and the description related prefix expansion)*; and

b) means (processor) for setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes (*column 8, Figures 5-8 and the description on right column related to prefix capture*).

Regarding **claim 12**, in accordance with Srinivasan reference entirety, Srinivasan discloses apparatus for encoding a plurality of predefined codes into a search key (*Figure 13*), the apparatus comprising a processor circuit (*processor or forwarding engine*) configured to:

a) produce a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predefined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations (*columns 7-8, Figures 5-8 and the description related prefix expansion)*, and

b) set bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes (*page 4, Figure 1 and the description on right column related to prefix capture*).

Regarding **claim 13**, in addition to features recited in base claim 12 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to arrange said bit positions in order by ascending lengths of corresponding said possible bit combinations (*see Figure 8*).

Regarding **claim 14**, in addition to features recited in base claim 13 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to further arrange said bit positions in order of ascending numeric value of corresponding said possible bit combinations (*see Figure 8*).

Regarding **claim 15**, in addition to features recited in base claim 12 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet (*see Figure 8; Link or Figure 9; pointer from root to leaves nodes*).

Regarding **claim 16**, in addition to features recited in base claim 12 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a plurality' of PNBAS, each PNBA corresponding to a subgroup of bits of said pre-defined codes (*see, Figure 8; Expanded prefixes*).

Regarding **claim 17**, in addition to features recited in base claim 16 (*see rationales discussed above*), Srinivasan further discloses wherein said processor

circuit is configured to produce an External Subtree Root Bit Array (ESRBA) for each PNBA said ESRBA having bit positions corresponding to possible further subgroups of bits of said pre-defined codes (*Figure 9; Expanded trie*).

Regarding **claim 18**, in addition to features recited in base claim 17 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a plurality of pages, each page comprising a plurality of PNBA-ESRBA pairs (prefix, length) (*see Figure 8 or Figure 9; Expanded trie*).

Regarding **claim 19**, in addition to features recited in base claim 17 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to produce a next hop array associating bit positions of said PNBA which have active bit with routing information for use by a router to route a packet (*see Figure 8; Link or Figure 9; Expanded trie and pointers*).

Regarding **claim 20**, in addition to features recited in base claim 19 (*see rationales discussed above*), Srinivasan further discloses wherein said processor circuit is configured to associate with each of said PNBAS a next hop pointer pointing to a position in said next hop array at which next hop information associated with a first active bit of said PNBA is located (*see Figure 9; Expanded trie and pointers*).

Regarding **claim 21**, in addition to features recited in base claim 20 (*see rationales discussed above*), Srinivasan further discloses wherein said processor is configured to arrange said plurality of PNBAS into a plurality of respective pages, each page comprising a PNBA, an associated ESRBA, an associated

next hop pointer and a next page pointer pointing to a next page in said plurality of respective page to be searched (*see Figure 9; Expanded trie and pointers*).

As per **claims 71-72**, they're rejected by the same rationales applied to claim 1.

Response to Arguments

4. Applicant's arguments filed 5/20/04 have been fully considered but they are not persuasive. Applicant's arguments will be addressed hereinbelow in the order in which they appear in the response filed 05/20/04.

In the Remarks of the outstanding response, on page 9 continue to page 10, pertaining the rejection of claim 1, Applicant argues "Srinivasan fails to discloses "*producing a PNBA having a plurality of bit positions corresponding to possible bit combinations of a bit string ... arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations and setting bits active in bit positions which corresponding to bit combinations of said possible bit combinations identified by said pre-defined codes .... The Examiner is requested to take careful note of applicant's use of the terms "bit positions" and "possible bit combination..." and the correspondence they have in applicant's claims. There is no teaching of any correspondence between a bit position and a bit combination in the Srinivasan reference*".

In response Examiner respectfully disagrees. As clearly pointed out in the Office Action, on page 4, section 4.1, left column, Srinivasan clearly discloses the original prefix on the left of Fig. 1 and the Controlled Prefix Expansion depicted

on the right of Fig. 1 corresponding to the broadly claimed limitation of "producing a PNBA (Expanded) having a plurality of bit positions corresponding to possible bit combinations of bit string (*Fig. 1; original P5=0* get expanded P5=00* and 01**) ... arranged by the length of said possible bit combinations and by numeric value of said bit combinations (Fig. 1; Length 2, 5 and 7) and setting bits active in bit possible which corresponding to bit combinations of said possible bit combinations identified by said pre-defined codes (*page 4, Fig. 1 and description on the right column relating to existing prefix captures*). The claim is not drafted in a means plus function nor a method step plus function and the claimed terms "bit positions" and "possible bit combination" are neither specifically defined in the claim nor the specification. Thus, they are subjected to Examiner's broadest reasonable interpretation consisting with the specification.

In the Remarks, on page 10 continue to page 11, pertaining the rejection of claim 2, Applicant argues Srinivasan reference does not teach the claimed limitation of "*arranging said bit positions in order by ascending lengths of corresponding said possible bit combinations*" because "*the expansion prefixes of Srinivasan are not equivalent to the PNBA recited in applicant's because for one reason, the bit positions in the expanded prefixes of Srinivasan do not corresponding to possible bit combinations*".

In response Examiner respectfully disagrees. Examiner asserts in the present condition, the claimed limitation in claim 2 is clearly anticipated by Srinivasan. Moreover, Examiner would like to emphasize that limitations in the claim are subjected to Examiner's broadest reasonable interpretation consisting

with the specification. On page 4, Fig. 4, Srinivasan clearly shows the expanded prefixes are arranged in an ascending length (Length 2, Length 5 and Length 7, respectively); thus, clearly reads on the claimed limitation in a manner set forth as claimed. Perhaps Applicant refers to a certain, novel and unobvious way that the PNBA are produced and arranged in the specification in making the contention that the Srinivasan reference fails to show certain feature of Applicant's invention. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. *See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).*

In the Remarks, on pages 11-13, pertaining the rejection of claim 4 and claim 5 and claim 6-10, Applicant states "*Examiner relies on Figure 8, Link or Figure 9 (?) and pointer from route to leave (?). Since Srinivasan has no Figures 8 or 9, applicant assumes the Examiner .... Applicants respectfully requests the Examiner to clarify this rejection with reference to the specific page and column(s) of Srinivasan that explicitly or inherently describe the subject matter claimed by applicant in claim 4*".

In response Examiner asserts there is neither typo nor mistake in the Office Action mailed 02/25/04. Claim 4 is rejected by Srinivasan non-patent literature (Office Action, page 5) and Srinivasan (US Patent 6,011,795) (Office Action, page 11). Perhaps the Applicants misread the Office Action mailed 02/25/2004 in demanding the Examiner's further explanation of the applied reference. The response is applied to argument pertaining claims 5-10.

As per arguments pertaining the rejection under 35 USC 102(e) of claims 1-21 as being anticipated by Srinivasan (US Patent 6,011,795). Please refer to the rationales discussed above as responses.

Examiner believes an earnest attempt has been made in addressing all of the Applicant's arguments. Due to the arguments are not persuasive and the amendment neither place the application in a favorable condition for allowance nor overcome the applied art of Srinivasan, the rejection from last Office Action is maintained.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Frank Duong whose telephone number is (703) 308-5428. The examiner can normally be reached on 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (703) 308-5463. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Frank Duong
Examiner
Art Unit 2666

August 5, 2004